(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 854 500 A1

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication
22.07.1998 Bulletin 1998/30

(51) Int Cl.[6]: **H01L 21/304**, H01L 21/762

(21) Application number: **98300107.4**

(22) Date of filing: **08.01.1998**

(84) Designated Contracting States:
AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **17.01.1997 JP 17685/97**

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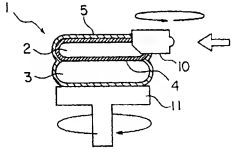
(54) Method of manufacturing a bonding substrate

(57) A method of manufacturing a bonding substrate is disclosed. An oxide film is formed on at least one of two semiconductor substrates, and the two substrates are brought into close contact with each other via the oxide film. The substrates are heat-treated in an oxidizing atmosphere in order to firmly join the substrates together. Subsequently, the peripheral portion of a device-fabricating substrate is ground to a predetermined thickness, and an unjoined portion at the periphery of the device-fabricating substrate is completely removed through etching. The device-fabricating substrate is then ground and/or polished in order to reduce the thickness of the device-fabricating substrate to a desired thickness. The step of grinding the peripheral portion of the device-fabricating substrate to a predetermined thickness is performed by relative and radial movement of a grinding stone from the peripheral portion of the substrate toward the center thereof. The method enables grinding of a peripheral portion of the device-fabricating substrate for the purpose of removing an unjoined portion such that the device-fabricating substrate is ground to as small a thickness as possible in order to increase productivity while reducing costs. The method also prevents damage from reaching the support substrate even when the device-fabricating substrate is ground to such a small thickness.

FIG. 2



EP 0 854 500 A1

Description

BACKGROUND OF THE INVENTION

Field of the Invention.

The present invention relates to a method of manufacturing a bonding substrate composed of two substrates bonded together, and more particularly to a method of manufacturing a so-called bonding SOI (Silicon on Insulator) substrate in which two silicon monocrystalline substrates, or a silicon monocrystalline substrate and an insulator substrate are bonded together via a silicon oxide film.

Description of the Related Art

There have been known various methods of manufacturing a bonding SOI substrate in which two silicon monocrystalline substrates are bonded together via a silicon oxide film. In the method shown, for example, in Japanese Patent Publication *(kokoku)* 5-46086, an oxide film is formed on at least one of two substrates, the two substrates are brought into close contact with each other with no foreign substance being interposed between the joint surfaces thereof; and the substrates are then subjected to heat treatment at a temperature of about 200 to 1200 °C in order to increase joint strength.

Since a bonding substrate whose joint strength has been increased by means of thermal treatment can undergo a subsequent grinding and polishing process, the thickness of one substrate on which devices are to be fabricated can be reduced to a desired thickness through grinding or polishing in order to obtain an SOI layer for formation of semiconductor device.

However, it is known that a bonding substrate manufactured in the above-described manner has an unjoined portion in an area extending about 1 - 3 mm from the peripheral edge of the substrate. In order to remove such an unjoined portion, there have been developed various techniques such as those shown in Japanese Patent Application Laid-Open *(kokai)* Nos. 3-89519, 4-263425, 3-250616, and 64-89346.

Although these methods can remove such an unjoined portion, they have the following drawbacks. In the techniques disclosed in Japanese Patent Application Laid-Open Nos. 3-89519 and 4-263425 in which the peripheral portion of one substrate on which devices are to be fabricated (bond wafer) is ground to reach the other substrate which serves as a support substrate (base wafer), the shape of the base wafer changes greatly from the original shape. In the technique disclosed in Japanese Patent Application Laid-Open No. 3-250616 in which a piece of masking tape is applied to a wafer to cover the entire wafer except the peripheral portion, and then etching is performed in order to remove the unjoined portion at the periphery of the wafer, the process becomes complicated. In the technique disclosed in Japanese Patent Application Laid-Open No. 64-89346 in which the entire peripheral portion of a bonded wafer is removed through etching, the production requires a prolonged period of time and high costs and the productivity is low.

In order to solve these problems, there has been proposed another method of manufacturing a boding substrate as disclosed in Japanese Patent Application Laid-Open *(kokai)* No. 7-45485. In this method, an oxide film is formed on the surface of at least one of two wafers (bond and base wafers); the two wafers are brought into close contact with each other via the oxide film; the wafers are heat-treated in an oxidizing atmosphere in order to firmly join the wafers together; an unjoined portion at the periphery of the bond wafer is completely removed; and the bond wafer is ground/polished to a desired thickness, wherein the complete removal of the unjoined portion at the periphery of the bond wafer is carried in such a way that the peripheral portion of the bond wafer is first removed through grinding to a thickness such that damage does not reach the base wafer, and the unjoined portion at the periphery of the bond wafer is completely removed through etching.

The above-described methods has advantages that shape of the base wafer is not changed, that masking tape or the like is not required to be used, and that the process does not become complicated unreasonably.

However, when the unjoined portion at the peripheral portion of the bond wafer is removed through grinding, damage may reach the base wafer unless the grinding is stopped such that the unjoined portion still has a considerably large thickness. If damage reaches the base wafer, there arises a problem that when the unjoined portion at the periphery of the bond wafer is completely removed by subsequent etching, etchant may reach the surface of the base wafer via the damaged buried oxide layer and form a scratch or depression in the surface, thereby decreasing yield in the subsequent device-fabrication step.

If the grinding amount of the peripheral portion of the bond wafer is decreased, the above-described problem can be solved. However, in this case, an amount of etching stock removal increases and therefore the etching process requires a prolonged period of time and increased costs such as that of etchant, thereby losing the advantage of mechanical grinding. From this, it may be concluded that the above-described method in which the entire peripheral edge of the bond wafer is removed through etching is preferable because of its fewer number of process steps.

SUMMARY OF THE INVENTION

The present invention has been accomplished to solve the above-mentioned problems, and an object of the invention is to provide a method of manufacturing a bonding substrate, which method enables grinding of a peripheral portion of a bond wafer for the purpose of re-

moving an unjoined portion such that the bond wafer is ground to as small a thickness as possible in order to increase productivity while reducing costs, and which method prevents damage from reaching a base wafer even when the bond wafer is ground to such a small thickness.

To achieve the above object, the present invention provides a method of manufacturing a bonding substrate, the method comprising the steps of forming an oxide film on at least one of two semiconductor substrates; bringing the two substrates into close contact with each other via the oxide film; heat-treating the substrates in an oxidizing atmosphere in order to firmly join the substrates together; grinding the periphery of a substrate on which a device is to be fabricated (hereinafter referred to as the "device-fabricating substrate") to a predetermined thickness, completely removing an unjoined portion at the periphery of the device-fabricating substrate through etching, and grinding and/or polishing the device-fabricating substrate in order to reduce the thickness of the device-fabricating substrate to a desired thickness, wherein the step of grinding the peripheral portion of the device-fabricating substrate to a predetermined thickness is performed by relative and radial movement of a grinding stone from the peripheral portion of the substrate toward the center thereof.

When the grinding of the peripheral portion of the device-fabricating substrate to a predetermined thickness is performed by relative and radial movement of a grinding stone from the peripheral portion of the substrate toward the center thereof as described above, damage in the direction of thickness of the wafer decreases, so that the bond wafer can be ground to a small thickness without generation of damage in the base wafer.

The present invention also provides a method of manufacturing a bonding substrate, the method comprising the steps of bringing a semiconductor substrate and an insulator substrate into close contact with each other; heat-treating the substrates in an oxidizing atmosphere in order to firmly join the substrates together; grinding the peripheral portion of the semiconductor substrate to a predetermined thickness; completely removing an unjoined portion at the periphery of the semiconductor substrate through etching; and grinding and/or polishing the semiconductor substrate in order to reduce the thickness of the semiconductor substrate to a desired thickness, wherein the step of grinding the peripheral portion of the semiconductor substrate to a predetermined thickness is performed by relative and radial movement of a grinding stone from the peripheral portion of the substrate toward the center thereof.

As described above, the present invention can be applied not only to the case where two semiconductor substrates are joined but also to the case where a semiconductor substrate and an insulator substrate are joined together and removed the unjoined portion at the peripheral portion of the semiconductor substrate in order to manufacture a bonding substrate.

In the methods according to the present invention, the grinding of the peripheral portion of the semiconductor substrate is preferably performed such that the thickness of the device-fabricating substrate is reduced to a thickness of 20 - 150 microns.

As described above, in the present invention, the substrate serving as a bond wafer can be ground to a thickness of 20 - 150 microns without generation of damage in the substrate serving as a base wafer. Therefore, the time required for a successive etching process can be shortened, and a bonding substrate of high quality can be manufactured with high productivity and at low cost.

BRIEF DESCRIPTION OF THE DRAWING

FIGS. 1A - 1G are diagrams illustrating a general process for manufacturing a bonding substrate according to the present invention;

FIG. 2 is an explanatory diagram showing the case where the peripheral portion of a bond wafer is ground to a predetermined thickness according to the present invention; and

FIGS. 3A and 3B are explanatory diagrams each showing the case where the peripheral portion of a bond wafer is ground to a predetermined thickness according to a conventional method.

DESCRIPTION OF THE PREFERRED EMBODIMENT

With reference to the drawing, an embodiment of the present invention will next be described for a case where two semiconductor substrates are joined together. However, the present invention is not limited thereto.

With reference to FIGS. 1A - 1G, the method according to the present invention will now be described step by step. First, material wafers (monocrystaline silicon mirror-polished wafers having a diameter of 5 inches and a <100> orientation, which are manufactured in accordance with, for example, the Czochralski method) are prepared as a bond wafer 2 and a base wafer 3 (FIG. 1A). Among the prepared silicon monocrystalline wafers, the bond wafer 2 is heat-treated such that an oxide film 4 is formed on the surface thereof (FIG. 1B).

Subsequently, the bond wafer 2 with the oxide film 4 is brought into close contact with the base wafer 3 in a clean atmosphere (FIG. 1C). The bond wafer 2 and the base wafer 3 are then heat-treated in an oxidizing atmosphere in order to firmly join the bond wafer 2 and the base wafer 3 so as to yield a bonding substrate 1. The heat treatment is performed at a temperature of 200 - 1200 °C in an atmosphere that contains oxygen or water vapor (FIG. 1D). At this time, the bond wafer 2 and the base wafer 3 are firmly joined together, and an oxide film 5 is formed on the entire outer surface of the bonding substrate 1. The oxide film 5 serves as an etching film in a subsequent step

In an area extending about 2 mm from the peripheral edge of the bonding substrate 1, the bond wafer 2 and the base wafer 3 have an unjoined portion. The unjoined portion must be removed because such an unjoined portion cannot be used as an SOI layer for fabrication of semiconductor devices, and may peel off in a subsequent process and cause various problems.

In order to remove the unjoined portion, as shown in FIG. IE, the peripheral portion of the bond wafer 2 where the unjoined portion exists is ground such that the thickness of the unjoined portion decreases to a predetermined thickness t. The grinding operation can remove the unjoined portion with high speed and high accuracy.

In this case, the predetermined thickness t is preferably made as small as possible in order to reduce the amount of etching stock removal in an etching step, which is subsequent to the step of removing the unjoined portion.

It is well known that when a silicon wafer is mechanically ground, mechanical damage is generated in the wafer, unlike the case of etching. Therefore, if the predetermined thickness t is reduced excessively, damage such as mechanical damage reaches the buried oxide layer 4 or the base wafer 3. In this case, when the unjoined portion at the periphery of the bond wafer 2 is completely removed by subsequent etching, etchant may reach the surface of the base wafer 3 via the damaged buried oxide layer 4 and form a scratch or depression in the surface, thereby decreasing the yield in the subsequent device-forming step.

Therefore, it is important to determine a way of grinding the peripheral portion of the bond wafer 2 to as small a thickness as possible without imparting damage to the buried oxide layer 4 or the base wafer 3.

Conventionally, as shown in FIGS. 3A and 3B, the peripheral portion of the bond wafer 2 is ground in such a way that a bonding wafer 1 is fixedly supported on a rotatable stage 11 which is then rotated, and a rotating grinding wheel 10 is caused to approach the bond wafer 2 from above (i.e., from the main-face side) in order to grind the peripheral portion of the bond wafer 2 in the thicknesswise direction of the substrate.

However, as a result of experimental studies performed by the inventors of the present invention, it was found that when the grinding wheel 10 is pressed against the bond wafer 2 in the thicknesswise direction of the wafer, damage caused by grinding is likely to be generated in the advancing direction of the grinding wheel 10, and therefore the buried oxide layer 4 or the surface of the base wafer 3 is apt to be damaged. Therefore, in the conventional method, the amount of the bond wafer 2 removed by grinding must be restricted such that the ground portion of the bond wafer 2 has a thickness of at least 150 microns as a predetermined thickness t.

If the ground portion of the bond wafer 2 has a thickness of 150 microns or more, an amount of etching stock removal by a subsequent etching process becomes larger, and therefore the etching process requires a prolonged period of time (e.g., 4 hours or more) and increased costs such as that of etchant, thereby losing the advantage of mechanical grinding.

Therefore, in the present invention, in order to grind the peripheral portion of the bond wafer 2 to a predetermined thickness t, the grinding wheel 10 is moved radially in relation to the bond wafer 2 such that, as shown in FIG. 2, the grinding wheel 10 moves from the peripheral portion toward the center of the bond wafer 2.

In this case, while heights of the bonding substrate 1 and the grinding wheel 10 and distance therebetween are maintained constant and the bonding substrate 1 and the grinding wheel 10 are rotated in opposite directions by unillustrated rotation mechanisms, the grinding wheel 10 is moved horizontally by an unillustrated feed mechanism in order to grind the peripheral portion of the bond wafer 2 toward the center portion of the wafer. Conversely, the stage 11 may be moved horizontally by an unillustrated feed mechanism while the position of the grinding wheel 10 is fixed, in order to press the peripheral portion of the bond wafer 2 against the grinding wheel 10.

The predetermined thickness t of the ground peripheral portion of the bond wafer 2 can be controlled through adjustment of the positional relationship between the grinding wheel 10 and the bond wafer 2 in the vertical direction.

In the present invention, the predetermined thickness t can be set to fall within the range of 20 - 150 microns through adjustment of the positional relationship between the grinding wheel 10 and the bond wafer 2 in the vertical direction.

In the present invention, since the bond wafer 2 is ground from the periphery toward the center of the bond wafer 2, damage is generated in a direction toward the center of the wafer, which is the advancing direction of the grinding wheel, so that damage is hardly generated in the thicknesswise direction.

Therefore, even when the peripheral portion of the bond wafer 2 is ground to a thickness as small as 20 - 150 microns, damage does not reach the buried oxide layer 4 or the base wafer 3.

Although the degree of damage generated toward the center of the bond wafer 2 increases, the problem can be solved through reduction in the width w of the peripheral portion of the bond wafer 2 to be ground by the grinding wheel 10 and removal of the generated damage through etching in a subsequent step.

In this way, the method of the present invention enables the peripheral portion of the bond wafer 2 to be ground to a thickness as small as 20 - 150 microns, without imparting damage to the buried oxide layer 4 or the base wafer 3.

However, even when the wafer is radially ground from the periphery thereof, damage of approximately 10 microns is generated in the thicknesswise direction of

the wafer. Therefore, if the wafer is ground to a thickness less than 20 microns, there arises a possibility that the base wafer 3 may be damaged. Therefore, such excessive grinding is not preferred.

Subsequently, as shown in FIG. 1F, the unjoined portion at the periphery of the bond wafer 2 is completely removed through etching. This etching can be performed through immersion of the bonding wafer 1 into an etchant whose etching speed for silicon monocrystal is greatly higher that that for oxide film. That is, although the peripheral portion of the bond wafer 2 is etched by the etchant because the silicon has been exposed through grinding, the remaining portions of the bonding substrate 1 are not etched because these portions are covered by the oxide film 5. An example of etching that exhibits selectivity is alkali etching utilizing KOH, NaOH, or the like.

In the present invention, since the thickness of the peripheral portion of the bond wafer 2 is sufficiently reduced, the unjoined portion at the periphery of the bonding substrate 1 can be completely removed in a short period of time through etching.

Finally, as shown in FIG. 1G, the surface of the bond wafer 2 is ground and/or polished in an ordinary manner in order to reduce the thickness of the bond wafer 2 to a desired thickness. Thus, a bonding substrate having an SOI layer 6 is manufactured.

EXAMPLES

Next, descriptions will be given of an example of the present invention and a comparative example.

(Example and Comparative Example)

Twenty mirror-polished CZ substrates having a diameter of 125 mm (5 inches) and a thickness of 625 microns (conductive type: p type; resistivity: 4 - 6 Ω . cm) were prepared and divided into 10 bond wafers and 10 base wafers. These wafers were joined in accordance with the processes shown in FIGS. 1A - 1D in order to yield 10 bonding substrates as shown in FIG. 1D.

For five of the thus-manufactured bonding substrates, as shown in FIG. 2, the peripheral portion of each wafer was radially ground from the periphery toward the center of the wafer (Example). Meanwhile, for the remaining five bonding substrates, as shown in FIG. 3A, the peripheral portion of each wafer was ground in the thicknesswise direction of the wafer (Comparative Example).

The grinding was performed through use of a #800 diamond grinding wheel, which was rotated at a peripheral speed of 1600 m/min in the direction opposite to that of the wafer, which was rotated at a peripheral speed of 300 mm/min. The grinding was performed through the advancing speed of 0.6 mm/min. The peripheral portion of the bond wafer radially extending over about 3 mm was ground until the thickness of the peripheral portion became 100 microns. The above-described conditions apply to both the Example and the Comparative Example, which differed only in the advancing direction of the grinding wheel.

The ten bonding wafers whose bond wafers had ground peripheral portions were immersed into a solution of 50% NaOH at 70 °C for about 3.5 hours, which was a condition for etching a silicon monocrystalline of a thickness of about 130 microns, in order to completely remove the unjoined portion at the periphery of the wafer.

Subsequently, ordinary grinding/polishing was carried out for the bonding wafers to complete the manufacture of a bonding substrate having an SOI layer of 2 micron thickness as shown in FIG. 1G.

Scratches existing on the surface the terrace portion 7 of the base wafer 3 of each of the ten thus-manufactured SOI substrates were counted through use of an optical microscope.

Although 20 - 50 scratches were observed in each of the wafers that had been ground by the method of the Comparative Example (conventional method), scratches that were considered to stem from grinding were not detected in the wafers that had been ground by the method according to the present invention.

The present invention is not limited to the above-described embodiment. The above-described embodiment is a mere example, and those having the substantially same structure as that described in the appended claims and providing the similar action and effects are included in the scope of the present invention.

In the above-described embodiment, a description is focused on the case where two semiconductor substrates are joined together in order to manufacture a bonding substrate. However, the present invention is also effective in removing peripheral unjoined portions that are produced in a manufacturing process in which a bonding substrate is manufactured through joining of a semiconductor wafer and an insulator substrate made of quartz, silicon carbide, silicon nitride, alumina, sapphire, or other ceramic materials.

Claims

1. A method of manufacturing a bonding substrate which comprises the steps of forming an oxide film on at least one of two semiconductor substrates, bringing the two substrates into close contact with each other via the oxide film; heat-treating the substrates in an oxidizing atmosphere in order to firmly join the substrates together; grinding the peripheral portion of a device-fabricating substrate to a predetermined thickness; completely removing an unjoined portion at the periphery of the device-fabricating substrate through etching; and grinding and/or polishing the device-fabricating substrate in order to reduce the thickness of the device-fabricating

substrate to a desired thickness, characterized in that said step of grinding the peripheral portion of the device-fabricating substrate to a predetermined thickness is performed by relative and radial movement of a grinding stone from the peripheral portion of the substrate toward the center thereof

2. A method of manufacturing a bonding substrate, the method comprising the steps of bringing a semiconductor substrate and an insulator substrate into close contact with each other, heat-treating the substrates in an oxidizing atmosphere in order to firmly join the substrates together, grinding the peripheral portion of the semiconductor substrate to a predetermined thickness; completely removing an unjoined portion at the periphery of the semiconductor substrate through etching; and grinding and/or polishing the semiconductor substrate in order to reduce the thickness of the semiconductor substrate to a desired thickness, characterized in that said step of grinding the periphery of the semiconductor substrate to a predetermined thickness is performed by relative and radial movement of a grinding stone from the peripheral portion of the substrate toward the center thereof

3. A method of manufacturing a bonding substrate according to Claim 1, characterized in that said grinding of the peripheral portion of the semiconductor substrate is performed such that the thickness of the device-fabricating substrate is reduced to a thickness of 20 - 150 microns.

4. A method of manufacturing a bonding substrate according to Claim 2, characterized in that said grinding of the peripheral portion of the semiconductor substrate is performed such that the thickness of the semiconductor substrate is reduced to a thickness of 20 - 150 microns

FIG. 1A

FIG. 1B

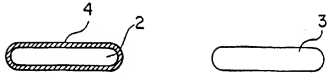


FIG. 1C

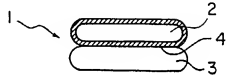


FIG. 1D

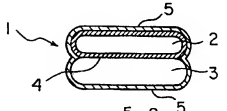


FIG. 1E

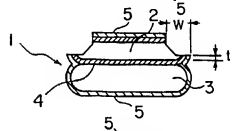


FIG. 1F

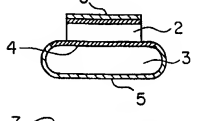


FIG. 1G

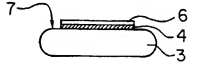


FIG. 2

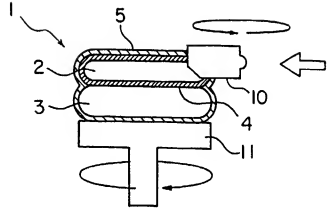


FIG. 3A

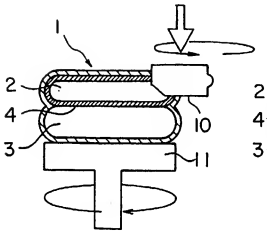
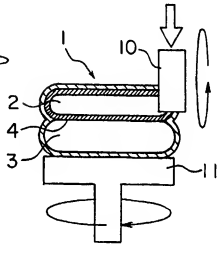


FIG. 3B



European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 98 30 0107

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
D,Y	PATENT ABSTRACTS OF JAPAN vol. 095, no. 005, 30 June 1995 & JP 07 045485 A (SUMITOMO SITIX CORP), 14 February 1995, * abstract *	1,2	H01L21/304 H01L21/762
Y	PATENT ABSTRACTS OF JAPAN vol. 009, no. 031 (E-295), 9 February 1985 & JP 59 175729 A (TOSHIBA KK), 4 October 1984, * abstract *	1,2	
A	PATENT ABSTRACTS OF JAPAN vol. 018, no. 507 (E-1609), 22 September 1994 & JP 06 176993 A (TOSHIBA CORP), 24 June 1994, * abstract *	1,2	
P,A	PATENT ABSTRACTS OF JAPAN vol. 097, no. 005, 30 May 1997 & JP 09 017984 A (SUMITOMO SITIX CORP), 17 January 1997, * abstract *	1,2	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	21 April 1998	Vancraeynest, F

CATEGORY OF CITED DOCUMENTS

X particularly relevant if taken alone
Y particularly relevant if combined with another document of the same category
A technological background
O non-written disclosure
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E earlier patent document, but published on, or after the filing date
D document cited in the application
L document cited for other reasons

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EPO FORM 1503 03.82 (P04C01)

(19) Europäisches Patentamt
European Patent Office
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(11) EP 0 935 280 A1

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
11.08.1999 Bulletin 1999/32

(51) Int Cl.[6]: **H01L 21/20**, H01L 21/762

(21) Application number: **99300620.4**

(22) Date of filing: **28.01.1999**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **04.02.1998 JP 2306698**
25.12.1998 JP 37031698

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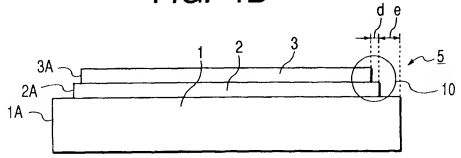
(54) SOI substrate and method of manufacturing the same

(57) A method of manufacturing a semiconductor substrate can effectively prevent a chipping phenomenon and the production of debris from occurring in part of the insulation layer and the semiconductor by removing a outer peripheral portion of the semiconductor substrate so as to make the outer peripheral extremity of the insulation layer to be located between the outer peripheral extremity of the semiconductor layer and that of the support member and hence the semiconductor layer and the insulation layer produce a stepped profile.

FIG. 1B



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